IN THE CLAIMS:

1. (Currently Amended) A phase locked loop circuit arrangement comprising an oscillator circuit controlled in response by a signal of a phase or frequency detection circuit, ~~said~~ phase locked loop circuit further comprising:

~~a)~~ first timer circuitry ~~means~~ for receiving a predetermined threshold frequency;

~~b)~~ second timer circuitry ~~means~~ for receiving an output frequency of said oscillator circuit, the first and second timing circuitries providing an output signal to indicate the status of the output frequency relative to the predetermined threshold frequency;

~~c)~~ change control circuitry ~~means~~ for generating a blocking signal in response to the outputs of said first and second timer circuitries ~~means~~, and

~~d)~~ blocking circuitry ~~means~~ for suppressing supply of said output signal towards said oscillator circuit in response to said blocking signal to stabilize the output frequency.

2. (Currently Amended) An arrangement according to claim 1, further comprising a reference oscillator circuit ~~means~~ for generating said threshold frequency.

3. (Currently Amended) An arrangement according to claim 1, wherein each of said first and second timer circuitries ~~means~~ comprise a counter circuit and wherein said threshold frequency and said output frequency are supplied to respective clock inputs of said counter circuits.

4. (Currently Amended) An arrangement according to claim 1, wherein said change control circuitry ~~means~~ comprises a finite state machine for receiving respective carry signals of said first and second timer circuitries ~~means~~, the finite state machine being configured to generate said blocking signal and a reset signal for resetting said first and second timer circuitries ~~means~~ in response to at least one of said carry signals.

5. (Currently Amended) An arrangement according to claim 4, wherein said finite state machine comprises a logic circuit adapted to generate a logic signal from which said

blocking signal is derived, and ~~an~~ wherein said logic signal is active when both carry signals are active, or when said reset signal and said blocking signal are active, or when said reset signal is not active and said blocking signal is active.

6. (Currently Amended) An arrangement according to claim 4, wherein said finite state machine has a first state during which said first and second timer circuitries ~~means~~ are operated and said blocking signal is not active, a second state during which said reset signal is active to reset said first and second timer circuitries ~~means~~ and said blocking signal is not active, a third state during which said first and second timer means are operated and said blocking signal is active, and a fourth state during which said reset signal is active to reset said first and second timer circuitries ~~means~~ and said blocking signal is active.

7. (Previously Presented) An arrangement according to claim 4, wherein said blocking signal and said reset signal are latched by respective flip-flop circuits to which said output frequency is supplied as a clock signal.

8. (Currently Amended) An arrangement according to claim 1, wherein said blocking means comprises controllable switching circuit configured ~~means~~ for switching a connection between said detection circuit and said oscillator circuit.

9. (Previously Presented) An arrangement according to claim 1, wherein said threshold frequency is an upper threshold frequency and said output signal is used to increase said output frequency of said oscillator circuit.

10. (Previously Presented) An arrangement according to claim 1, wherein said threshold frequency is a lower threshold frequency and said output signal is used to decrease said output frequency of said oscillator circuit.

11. (New) A phase locked loop circuit arrangement comprising:

a phase or frequency detection circuit providing a first signal;

an oscillator circuit controlled in response to the first signal;

a timing circuit configured to receive a predetermined threshold frequency and to receive an output frequency of the oscillator circuit and, in response thereto, provide a timing circuit output;

a change control circuit configured to generate a blocking signal in response to the output of the timing circuit; and

a blocking circuit configured to suppress supply of the timing circuit output towards the oscillator circuit in response to the blocking signal and, thereby, stabilize the output frequency of the oscillator circuit.

12. (New) The phase locked loop circuit arrangement of claim 11, wherein the timing circuit is further configured to indicate the status of the output frequency relative to the predetermined threshold frequency.

13. (New) The phase locked loop circuit arrangement of claim 11, wherein the change control circuit includes a finite state machine for responding to the timing circuit, the finite state machine being configured to generate the blocking signal and a reset signal for resetting the timing circuit in response thereto.